Please add the following new claim:

18. (new) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of wire bonds connecting pads on an integrated circuit chip to conductive leads,

a foamed polymer sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.

REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 1-17 were pending in this case. Non-elected Claim 17 has been cancelled. New Claim 18 has been added. Claims 1, 10, 11, 14, and 16 have been amended to more clearly define the claimed invention.

Claims 11 and 14 were objected to because of informalities. The claims have been amended in response to the objection.

Claims 1, 3, and 10-12 stand rejected under 35 U.S.C. 102(e) as being anticipated by Choi (U.S. Patent No. 6,013,109). Claim 1, as amended, includes the feature of "a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads." Choi does not disclose substantially parallel and closely-spaced wires. Claim 3 depends

from Claim 1 and is therefore patentable over Choi for at least the reasons presented above. Claim 10 includes the feature wherein "said device is packaged in a Ball Grid Array package." Choi does not disclose a device packaged in a Ball Grid Array package. Claim 11 depends from Claim 1 and is therefore patentable over Choi for at least the reasons presented above. Claim 12 includes the feature of "a semiconductor package having leads, a substrate, and a housing shell surrounding an open cavity." Choi does not disclose a housing shell surrounding an open cavity. Therefore, Applicants submits that Claims 1, 2, and 10-12 are patentable over Choi.

Claims 2, 4-9, and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Eysermans (U.S. Patent No. 4,048,670). Claim 2 depends from Claim 1. As stated above, Claim 1 includes the feature of "a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads." Neither Choi nor Eysermans disclose or suggest such a feature. Therefore, Applicant submits that Claim 1, and Claim 2 and 4-9 which depend therefrom, are patentable over the combined references. Claim 16, as amended, includes the feature of "a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads." Both Choi and Eysermans teach away from this claimed feature by covering chip, leadframe, and other package components in addition to wires or portions of wires.

Claims 14 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Featherby, et al. (U.S. Patent No. 6,368,899). Claims 14 and 15 depend from Claim 1. Claim 1 is distinguishable from Choi for the reasons presented above. Featherby does not cure the deficiencies of Choi. In Featherby's Figure 12, note that bond wires 18 are not substantially parallel or closely-spaced to the extent that mutual capacitance would be significant.

Claims 14 and 15 depend from Claim 1 and are therefore patentable over Choi in view of Featherby for the reasons presented above. In addition, Claim 14 includes the feature wherein "said cavity package shell comprises ceramic." The Examiner refers to Featherby's Figure 8 as including a cavity package shell. However, at col. 12, lines 10-15, Featherby refers to element 12 as a plastic package. It is therefore clear that the package of Figure 8 is simply a plastic package with a duplex coating, and is not a cavity package. The same reasoning applies to the rejection of Claim 15. Featherby does not disclose or suggest a cavity package.

New Claim 18 includes features of Claims 1-16 that are indicated above to make those claims patentable over the references of record. Therefore, Applicant respectfully requests that Claim 18 be passed to issuance along with Claims 1-16.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-16 and 18. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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In th Claims:

Please amend the claims as follows:

1. (amended) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads,

a low dielectric constant sheath surrounding each wire, and

a mold compound encasing the chip, sheathed wires, and leads.

10. (amended) A device as in claim 1 wherein said device is packaged in [as] a Ball Grid Array package.

11. (amended) A device as in claim 1 wherein said device is packaged [packages] as a leaded surface mount package.

14. (amended) A device as in claim 1 wherein said cavity package shell comprises a ceramic.

16. (amended) [An insulated wire bond including a conductive wire and a sheath of foamed polymer] A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of wire bonds connecting pads on an integrated circuit chip to conductive leads,

a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.

17. (cancelled without prejudice).

Please add the following new claim:

18. (new) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of wire bonds connecting pads on an integrated circuit chip to conductive leads,

a foamed polymer sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.